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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/825,357	04/16/2004	Dai Yun Lee	8733.1031.00-US	8106

30827 7590 03/24/2010

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EXAMINER	
LAM, VINH TANG	
ART UNIT	PAPER NUMBER
2629	
MAIL DATE	DELIVERY MODE
03/24/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/825,357	LEE ET AL.	
	Examiner	Art Unit	
	VINH T. LAM	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 January 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) *1-3,6,24 and 25* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4,5 and 7-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim **12** is objected to because of the following informalities: Typographical error.

"...while the remaining control thin film transistor is provided at the **(i+1)the** horizontal line..." should be "...while the remaining control thin film transistor is provided at the **(i+1)th** horizontal line...".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the **first paragraph** of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim **19** is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Regarding Claim **19**, the speciation as originally filed has failed to provide support for the recitation of "...wherein ***each of the gate lines is shared*** with the pixels positioned adjacently to each other ***at the upper and lower sides of the gate line*** ...".

The specification does not reasonably convey one skill in the art how to make or use applicant claimed invention for "...wherein ***each of the gate lines is shared*** with the pixels positioned adjacently to each other ***at the upper and lower sides of the gate line*** ...".

The following is a quotation of the **second paragraph** of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim **19** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The limitation of Claim **19** "...wherein ***each of the gate lines is shared*** with the pixels positioned adjacently to each other ***at the upper and lower sides of the gate line*** ..." is not clear.

What does "...wherein ***each of the gate lines is shared*** with the pixels positioned adjacently to each other ***at the upper and lower sides of the gate line*** ..." mean?

According to the Specification and specifically FIG. 6, each of the gate lines, GLi or GLi+2 for example, is ***NOT*** shared with the pixels positioned adjacently to each other at the upper and lower sides of the gate line.

The above limitation is not only rejected under 35 U.S.C. 112 2nd ¶ but also invoked 35 U.S.C. 112 1st ¶ since there is no disclosure of "...wherein ***each of the gate***

lines is shared with the pixels positioned adjacently to each other ***at the upper and lower sides of the gate line*** ..." in the originally filed specification.

To further advance prosecution, the Examiner interprets the above limitation in agreement with the Specification and Drawing.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) a patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims **4-23** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Inukai (US Pub. 2002/0000576)** in view of **Komiya (US Patent US 6924602).**

Regarding Claim **4**, (Currently Amended) **Inukai** teaches an electro-luminescence display device, comprising:

electro-luminescence cells (***[0070]***, *FIG.* ***1***, *i.e. pixel portion* ***101***) arranged in a matrix type ([**0075**], FIG. **2**) at crossings of gate lines (***[0074]***, *FIG.* ***2***, *i.e.* ***G0-G(y+1)***) and data lines (***[0074]***, *FIG.* ***2***, *i.e.* ***S1-Sx***);

a supply voltage line for supplying a driving voltage to the electro-luminescence cells (***[0074]***, *FIG.* ***2***, *i.e.* ***V1-Vx***);

driving circuits (***[0077]***, *FIG.* ***3***, *i.e.* ***105 & 107***) for controlling a current applied from the driving voltage of the supply voltage line to the electro-luminescence cells

([*0080*], *FIG.* ***3***) in response to video signals ([*0071*], *FIG.* ***1***), wherein each of driving circuit includes a first driving circuit and a second driving circuit ([*0077*], *FIG.* ***3***, *i.e.* ***105 & 107***) which are formed at horizontal lines different from each other ([*0077*], [*0078*], *FIG.* ***3***, *i.e.* ***Gi & G(i-1))***.

However, **Inukai** does not teach the control circuits applying video signals to and positioning between the driving circuits.

In the same field of endeavor, **Komiya** teaches

control circuits (*Col.* ***3***, *Ln.* ***44-58***, *FIG.* ***1***, *i.e. top (associated with Gate Line 1) and bottom (associated with Gate Line 2),* ***each*** *comprises* ***TFT3*** *and* ***TFT4***) for applying the video signals (*Col.* ***4***, *Ln.* ***1-9***, *FIG.* ***1***, *i.e.* ***Data Line 1****) to the driving circuits (Col.* ***3***, *Ln.* ***26-43***, *FIG.* ***1***, *i.e. top (associated with Gate Line 1) and bottom (associated with Gate Line 2),* ***each*** *comprises* ***TFT1***, ***TFT2***, ***capacitor***, *and an* ***EL***), wherein each of the control circuits is directly connected between the data line (*Col.* ***4***, *Ln.* ***1-9***, *FIG.* ***1***, *i.e.* ***Data Line 1***) and the supply voltage line (*Col.* ***3***, *Ln.* ***34-42***, *FIG.* ***1***, *i.e.* ***PVDD/VEE***) and is controlled by one of the gate lines (*Col.* ***3***, *Ln.* ***44-52***, *FIG.* ***1***, *i.e.* ***Gate Line 0***), and

wherein each of the control circuits (*Col.* ***3***, *Ln.* ***44-58***, *FIG.* ***1***, *i.e. top (associated with Gate Line 1) and bottom (associated with Gate Line 2),* ***each*** *comprises* ***TFT3*** *and* ***TFT4***) is positioned between the first driving circuit the second driving circuit (*Col.* ***3***, *Ln.* ***26-43***, *FIG.* ***1***, *i.e. top (associated with Gate Line 1) and bottom (associated with Gate Line 2),* ***each*** *comprises* ***TFT1***, ***TFT2***, ***capacitor***, *and an* ***EL***) so that the control circuit supplies the video signal to the first driving circuit and the second driving circuit (*FIG.* ***1***,

i.e. each control circuit supplies video signal independently and correspondingly to the top and bottom driving circuits).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine **Inukai** teaching of an electro-luminescence display device having gate lines, data lines, a supply voltage line, and driving circuits with **Komiya** teaching of control circuits connections to the driving circuits to effectively improve the aperture ratio and simultaneously to reduce the power consumption.

Regarding Claim **19**, (Currently Amended) **Inukai** teaches an electro-luminescence display device, comprising:

a plurality of pixels (***[0070]***, *FIG.* ***1***, *i.e. pixel portion* ***101***) arranged in a matrix type (***[0075]***, *FIG.* ***2***);

a plurality of data lines (***[0074]***, *FIG.* ***2***, *i.e.* ***S1-Sx***) for applying video signals to the pixels;

a plurality of gate lines (***[0074]***, *FIG.* ***2***, *i.e.* ***G0-G(y+1))*** crossing the data lines,

electro-luminescence cells provided for each pixel (***[0070]***, *FIG.* ***1***, *i.e. pixel portion* ***101***);

a supply voltage line for supplying a driving voltage to the electro-luminescence cells (***[0074]***, *FIG.* ***2***, *i.e.* ***V1-Vx***);

driving circuits (***[0077]***, *FIG.* ***3***, *i.e.* ***105 & 107***) for applying a current corresponding to the video signals to the electro- luminescence cells (***[0080]***, *FIG.* ***3***) in response to the video signals (***[0071]***, *FIG.* ***1***), wherein each of driving circuit includes a first driving circuit and a second driving circuit (***[0077]***, *FIG.* ***3***, *i.e.* ***105 & 107***) which are

formed at horizontal lines different from each other (***[0077]***, ***[0078]***, *FIG.* ***3***, *i.e.* ***Gi & G(i-1)***).

However, **Inukai** does not teach that each of the gate lines are share with pixels at the upper and lower and control circuits connections relative to the drive circuits.

In the same field of endeavor, **Komiya** teaches

each of the gate lines (*Col.* ***3***, *Ln.* ***44-52***, *FIG.* ***1***, *i.e.* ***Gate Line 0***) is shared with the pixels positioned adjacently to each other at the upper and lower sides of the gate line (*Col.* ***3***, *Ln.* ***26-43***, *FIG.* ***1***, *i.e. top (associated with Gate Line 1) and bottom (associated with Gate Line 2),* ***each*** *comprises* ***TFT1***, ***TFT2***, ***capacitor***, *and an* ***EL***);

control circuits (*Col.* ***3***, *Ln.* ***44-58***, *FIG.* ***1***, *i.e. top (associated with Gate Line 1) and bottom (associated with Gate Line 2),* ***each*** *comprises* ***TFT3*** *and* ***TFT4***) for applying the video signals (*Col.* ***4***, *Ln.* ***1-9***, *FIG.* ***1***, *i.e.* ***Data Line 1***) to the driving circuits (*Col.* ***3***, *Ln.* ***26-43***, *FIG.* ***1***, *i.e. top (associated with Gate Line 1) and bottom (associated with Gate Line 2),* ***each*** *comprises* ***TFT1***, ***TFT2***, ***capacitor***, *and an* ***EL***), wherein each of the control circuits is directly connected between the data line (*Col.* ***4***, *Ln.* ***1-9***, *FIG.* ***1***, *i.e.* ***Data Line 1***) and the supply voltage line (*Col.* ***3***, *Ln.* ***34-42***, *FIG.* ***1***, *i.e.* ***PVDD/VEE***) and is controlled by one of the gate lines (*Col.* ***3***, *Ln.* ***44-52***, *FIG.* ***1***, *i.e.* ***Gate Line 0***) and

wherein each of the control circuits (*Col.* ***3***, *Ln.* ***44-58***, *FIG.* ***1***, *i.e. top (associated with Gate Line 1) and bottom (associated with Gate Line 2),* ***each*** *comprises* ***TFT3*** *and* ***TFT4***) is positioned between the first driving circuit and the second driving circuit (*Col.* ***3***, *Ln.* ***26-43***, *FIG.* ***1***, *i.e. top (associated with Gate Line 1) and bottom (associated with Gate Line 2),* ***each*** *comprises* ***TFT1***, ***TFT2***, ***capacitor***, *and an* ***EL***) so that the control

circuit supplies the video signal to the first driving circuit and the second driving circuit (*FIG. **1**, i.e. each control circuit supplies video signal independently and correspondingly to the top and bottom driving circuits*).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine **Inukai** teaching of an electro-luminescence display device having gate lines, data lines, a supply voltage line, and driving circuits with **Komiya** teaching of control circuits connections to the driving circuits to effectively improve the aperture ratio and simultaneously to reduce the power consumption.

Regarding Claim **5**, (Previously Presented) the electro-luminescence display device according to claim 4, wherein **Inukai** teaches the first driving circuit is provided at the ith horizontal line (wherein i is an integer) to apply the current to the electro-luminescence cell positioned at the ith horizontal line, in response to a video signal from the control circuit controlled by the ith gate line, when a gate signal is applied to the (i-1)th gate line (*Col. **4**, **[0080]**, FIG. **3***), and

the second driving circuit is provided at the (i+1)th horizontal line to apply the current to the electro-luminescence cell positioned at the (i+1)th horizontal line, in response to a video signal from the control circuit controlled by the ith gate line, when a gate signal is applied to the (i+1)th gate line (*Col. **4**, **[0080]**, FIG. **3***).

Regarding Claim **7**, (Original) the electro-luminescence display device according to claim 5, wherein **Inukai** teaches the (i+1)th gate line is connected to a driving circuit provided at the (i+2)th horizontal line (*FIG. **2***).

Regarding Claim **8**, (Original) the electro-luminescence display device according to claim 5, wherein **Inukai** teaches the (i-1)th gate line (*FIG. **3**, i.e. **Gi***) is connected to a driving circuit (*FIG. **3**, i.e. **105***) provided at the (i-1)th horizontal line (*FIG. **3**, i.e. **Gi***).

Regarding Claim **9**, (Original) the electro-luminescence display device according to claim 5, wherein **Inukai** teaches the first driving circuits includes:

a first driving thin film transistor having a source terminal connected to the supply voltage line and a drain terminal connected to the electro-luminescence cell positioned at the ith horizontal line (*Col. **4**, **[0082]**, FIG. **3***);

a second driving thin film transistor having a drain terminal connected to a gate terminal of the first driving thin film transistor, a source terminal connected to the control circuit and a gate terminal connected to the (i-1)th gate line (*Col. **4**, **[0080]**, FIG. **3***); and

a storage capacitor connected between the source terminal and the gate terminal of the first driving thin film transistor (*Col. **4**, **[0081]**, FIG. **3***).

Regarding Claim **10**, (Original) the electro-luminescence display device according to claim 5, wherein **Inukai** teaches the second driving circuits includes:

a first driving thin film transistor having a source terminal connected to the supply voltage line and a drain terminal connected to the electro-luminescence cell positioned at the (i+1)th horizontal line (*Col. **4**, **[0082]**, FIG. **3***);

a second driving thin film transistor having a drain terminal connected to a gate terminal of the first driving thin film transistor, a source terminal connected to the control circuit and a gate terminal connected to the (i+1)th gate line (*Col. **4**, **[0080]**, FIG. **3***); and

a storage capacitor connected between the source terminal and the gate terminal of the first driving thin film transistor (*Col. **4**, **[0081]**, FIG. **3***).

Regarding Claim **20**, (Original) the electro-luminescence display device according to claim 19, **Inukai** further teaches comprising:

a gate driver for applying a gate signal having a turn-on potential during two horizontal periods to the gate lines (*Col. **7**, **[0124]**, **[0125]**, FIG. **5A***).

Regarding Claim **21**, (Original) the electro-luminescence display device according to claim 20, wherein **Inukai** teaches a gate signal applied to the ith gate line (wherein i is an integer) overlaps a gate signal applied to the (i+1)th gate line during one horizontal period (*Col. **7**, **[0124]**, **[0125]**, FIG. **5A***).

Regarding Claim **22**, (Original) the electro-luminescence display device according to claim 21, wherein **Inukai** teaches each of the driving circuits includes:

a first driving circuit provided at the ith horizontal line (wherein i is an integer) to apply the current to the electro-luminescence cell positioned at the ith horizontal line, in response to a video signal from the control circuit controlled by the ith gate line, when a gate signal is applied to the (i-1)th gate line (*Col. **4**, **[0082]**, FIG. **3***); and

a second driving circuit provided at the (i+1)th horizontal line to apply the current to the electro-luminescence cell positioned at the (i+1)th horizontal line, in response to a video signal from the control circuit controlled by the ith gate line, when a gate signal is applied to the (i+1)th gate line (*Col. **4**, **[0080]**, FIG. **3***).

Regarding Claim **23**, (Original) the electro-luminescence display device according to claim 22, wherein **Komiya** teaches one of the control circuits (*Col. **3**, Ln.*

44-58**, FIG. **1**, i.e. top (associated with Gate Line 1) and bottom (associated with Gate Line 2), **each** comprises **TFT3** and **TFT4**)* is positioned between the first driving circuit and the second driving circuit (*Col. **3**, Ln. **26-43**, FIG. **1**, i.e. top (associated with Gate Line 1) and bottom (associated with Gate Line 2), **each** comprises **TFT1**, **TFT2**, **capacitor**, and an **EL).

Regarding Claim **11**, (Original) the electro-luminescence display device according to claim 9 or 10, wherein **Komiya** teaches the control circuit includes:

a first control thin film transistor having a source terminal connected to the supply voltage line and a drain terminal and a gate terminal connected to the source terminal of the second driving thin film transistor (*Col. **3**, Ln. **34-44**, FIG. **1***); and

a second control thin film transistor having a drain terminal connected to the gate terminal of the first control thin film transistor, a source terminal connected to the data line and a gate terminal connected to the ith gate line (*Col. **3**, Ln. **34-44**, FIG. **1***).

Regarding Claim **12**, (Original) the electro-luminescence display device according to claim 11, wherein **Inukai** teaches any one of the first and second control thin film transistors is provided at the ith horizontal line while the remaining control thin film transistor is provided at the (i+1)th horizontal line (*Col. **4**, **[0079]**, **[0080]**, FIG. **3***).

Regarding Claim **13**, (Original) the electro-luminescence display device according to claim 11, **Inukai** further teaches comprising:

a gate driver for applying a gate signal having a turn-on potential during two horizontal periods to the gate lines (*Col. **7**, **[0124]**, **[0125]**, FIG. **5A***).

Regarding Claim **14**, (Original) the electro-luminescence display device according to claim 13, wherein **Inukai** teaches a gate signal applied to the ith gate line overlaps a gate signal applied to the (i+1)th gate line during one horizontal period (*Col. **7**, **[0124]**, **[0125]**, FIG. **5A***).

Regarding Claim **15**, (Original) the electro-luminescence display device according to claim 13, wherein **Inukai** teaches, if a gate signal is applied to the (i-1)th and ith gate lines, then the second driving thin film transistor connected to the (i-1)th gate line and the second control thin film transistor connected to the ith gate line are turned on (*Col. **4**, **[0079]**, **[0080]**, FIG. **3***); and

as the second control thin film transistor is turned on, a video signal from the data line is applied to the first driving thin film transistor and the first control thin film transistor that are positioned at the ith horizontal line (*Col. **4**, **[0079]**, **[0080]**, FIG. **3***).

Regarding Claim **16**, (Original) the electro-luminescence display device according to claim 15, wherein **Inukai** teaches the first driving thin film transistor positioned at the ith horizontal line applies the current corresponding to the video signal to the electro-luminescence cell provided at the ith horizontal line (*Col. **4**, **[0084]**, FIG. **3***).

Regarding Claim **17**, (Original) the electro-luminescence display device according to claim 15, wherein **Inukai** teaches the first control thin film transistor applies the current corresponding to the video signal from the supply voltage line to the data line (***[0080]***, *FIG. **3***).

Regarding Claim **18**, (Original) the electro-luminescence display device according to claim 17, wherein **Inukai** teaches a voltage corresponding to the current flowing in the first control thin film transistor is stored in the storage capacitor (*Col. **4**, **[0081]**, FIG. **3***).

Response to Arguments/Amendments/Remarks

5. Applicant's arguments, see Page(s) 8-11filed 01/14/2010, with respect to 35 U.S.C. § 103(a) have been fully considered and are not persuasive.

Applicant argues that the references do not teach "*...a first driving circuit and a second driving circuit are formed at horizontal lines different from each other, each of the control circuits is directly connected between the data line and supply voltage line, and is positioned between the first driving circuit and the second driving circuit so that the control circuit supplies the video signal to the first driving circuit and the second driving circuit...*". However, the Examiner respectfully disagrees because the Claim Limitations are substantially broad and do not specifically reflect the details of FIG. 6. Therefore, the ***combination of references*** are readable on the claimed invention, explicitly,

Teaches **Inukai** a first driving circuit and a second driving circuit (*[**0077**], FIG. **3**, i.e. **105 & 107***) which are formed at horizontal lines different from each other (*[**0077**], [**0078**], FIG. **3**, i.e. **Gi & G(i-1)***) and

Komiya teaches

each of the control circuits is directly connected between the data line (*Col. **4**, Ln. **1-9**, FIG. **1**, i.e. **Data Line 1***) and the supply voltage line (*Col. **3**, Ln. **34-42**, FIG. **1**, i.e. **PVDD/VEE***) and is controlled by one of the gate lines (*Col. **3**, Ln. **44-52**, FIG. **1**, i.e. **Gate Line 0***), each of the control circuits (*Col. **3**, Ln. **44-58**, FIG. **1**, i.e. top (associated with Gate Line 1) and bottom (associated with Gate Line 2), **each** comprises **TFT3** and **TFT4***) is positioned between the first driving circuit the second driving circuit (*Col. **3**, Ln. **26-43**, FIG. **1**, i.e. top (associated with Gate Line 1) and bottom (associated with Gate Line 2), **each** comprises **TFT1**, **TFT2**, **capacitor**, and an **EL***) so that the control circuit supplies the video signal to the first driving circuit and the second driving circuit (*FIG. **1**, i.e. each control circuit supplies video signal independently and correspondingly to the top and bottom driving circuits*).

Please refer to the above rejections for detail.

6. Claims **1-3**, **6**, and **24-25** are cancelled.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to VINH T. LAM whose telephone number is (571)270-3704. The examiner can normally be reached on M-F (7:00-4:30) EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on (571) 272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Vinh T Lam/
Examiner, Art Unit 2629

/Amare Mengistu/
Supervisory Patent Examiner, Art Unit 2629